Digital Frequency-locked Loop Design Strategies in the ASAP7 Open PDK

EE 241B Project Proposal

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Abstract

Energy- and area-efficient clock generation is essential for data sampling, processing, and wake-up timing in low-power internet-of-things (IoT) applications [1]. Digital frequency-locked loops (DFLLs) provide a convenient avenue for achieving this objective, as they allow for easy implementation of optimized loop calibration algorithms and structures, without analog design concerns such as strict supply voltage requirements, incorporation of large loop filter capacitors, and performance degradation due to issues of device mismatch and PVT variation that exist in advanced technology nodes [2].

Recent publications on DFLL design diverge from the standard DFLL architecture, which includes a digitally-controlled oscillator (DCO), time-to-digital converter (TDC), and digital loop filter (DLF) [2], through a number of design innovations. References 1 and 2 focus on ultra-low power applications, duty-cycling power to the locking circuitry once the DFLL frequency is settled [1] and operating the power-hungry DCO in the subthreshold region to achieve unprecedented energy efficiency [2]. On the other hand, references 3 and 4 harness the portability and scalability of synthesizable digital circuits by using a highly simplified design implemented directly in RTL [3] and an entirely standard-cell-based approach [4], resulting in a reusable block that can be easily integrated into digital synthesis flows and ported between technology nodes. Reference 5 seeks to push the performance of all-digital phase/frequency locking loops, accomplishing fast locking, low phase noise, low jitter, and large output frequency range by augmenting the traditional architecture with a dynamic gain adjustment unit.

After performing a comprehensive review of state-of-the-art literature, including the papers referenced above, we propose to implement a digital frequency-locked loop incorporating some of the aforementioned innovations using the ASAP7 free process design kit (PDK), before evaluating its performance against the prior art with regard to one of the above figures of merit: power, portability, or precision.

References

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