A Wide Tuning Range All-Digital Phase-Locked Loop with Fine Resolution for Digital Clock Generation in Predictive 7 nm FinFET Technology

Averal Kandala and Micah Roschelle

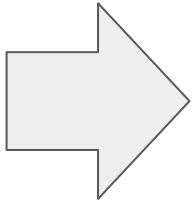
{averal, micah.roschelle}@eecs.berkeley.edu

PLLs: From Analog/Mixed-Signal to Digital

Traditional PLLs in Modern SoCs

- Low voltage headroom
- Wide PVT variation
- Digital interference
- Strict design rules
- SoC technology constantly changing

→ *Analog/mixed signal design is difficult in these conditions*

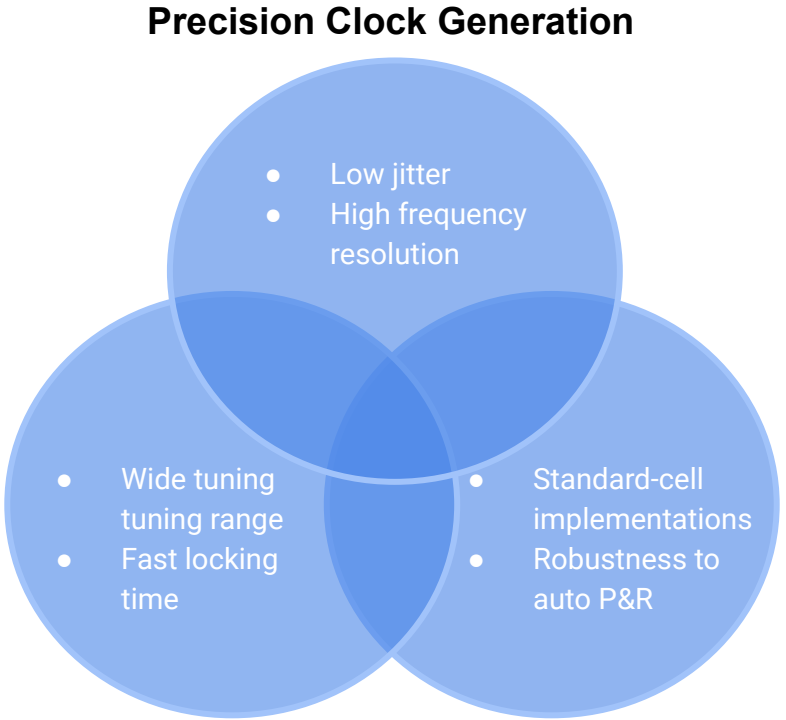


All-Digital PLL

- PVT and interference tolerant
- Easy portability between technologies through digital flow
- Easily programmable

But the translation to the digital domain brings its own challenges

Critical Challenges in State-of-the-Art ADPLL Design



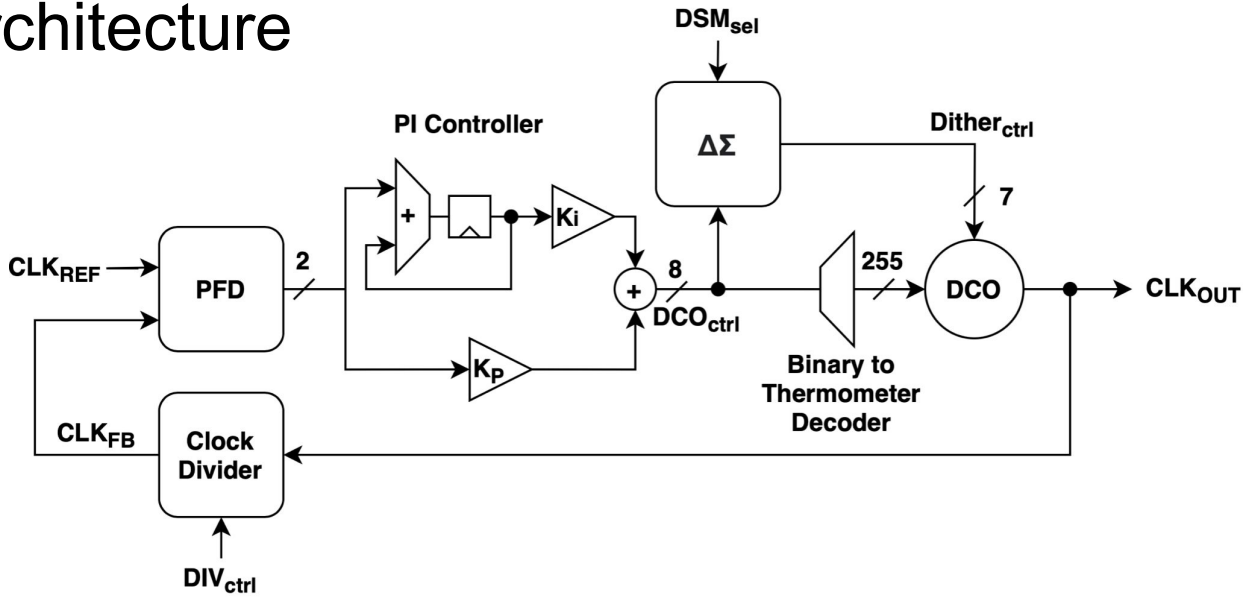
Proposed ADPLL Architecture

Design:

- DCO and DSM enable wide frequency range with fine output resolution

Implementation:

- *DCO:* Schematic-level design
- *PLL:* Verilog and logic synthesis



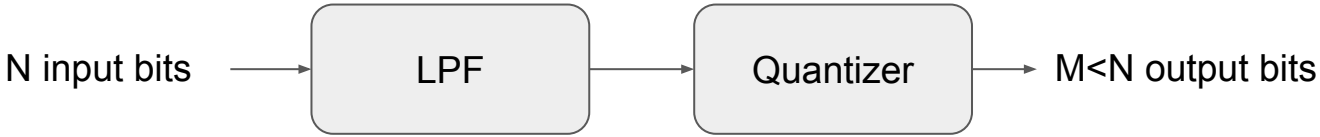
Key design parameters:

- CLK_{REF}= 500MHz
- Target CLK_{OUT}= 4GHz
- Divisor = 2,4,6,8
- $K_i=2^{-7}$, $K_P=2^0 \rightarrow$ PM=90°,ω_{UGBW}=1.4GHz
- Up to 3rd-order DSM for dithering
  - Fine resolution of ~9MHz
- 8-bit DCO, 0.5 - 7.24GHz @ 0.7V
- Coarse DCO Gain of 27MHz/LSB
- Supply scalable down to 0.3V

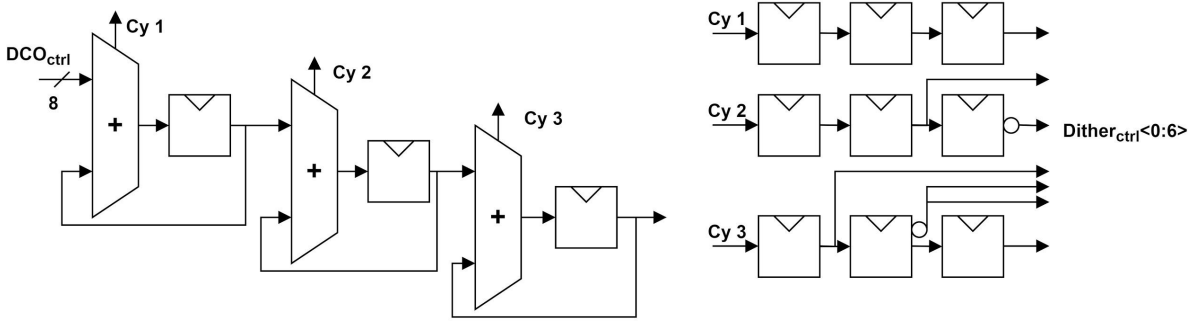
Dithering and DSM Concept

Grayscale implemented in a black-and-white image through dithering [1]

Idea: Mitigate quantization error and improve output resolution by introducing intermediate states that are selected pseudo-randomly

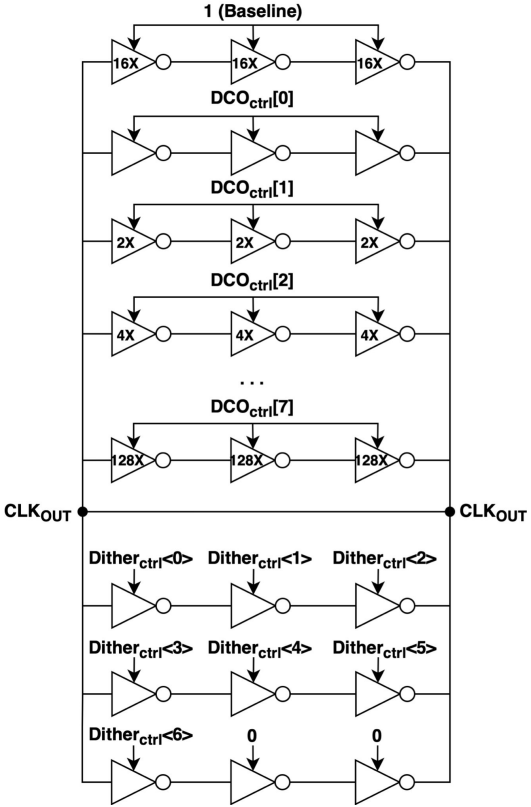


Implement programmable 3rd-order DSM to allow adaptive trade-off of fine resolution and low jitter



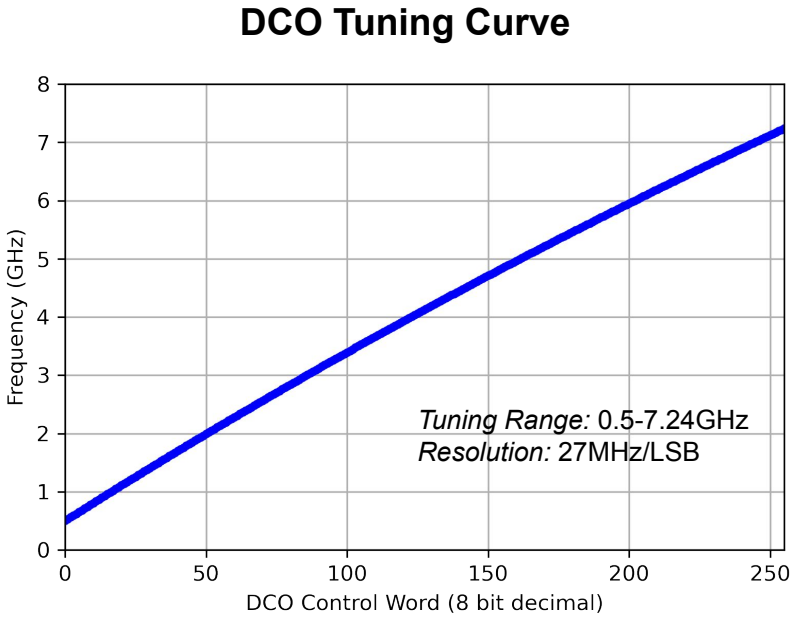
DCO for Wide Supply and Tuning Range, Low Jitter

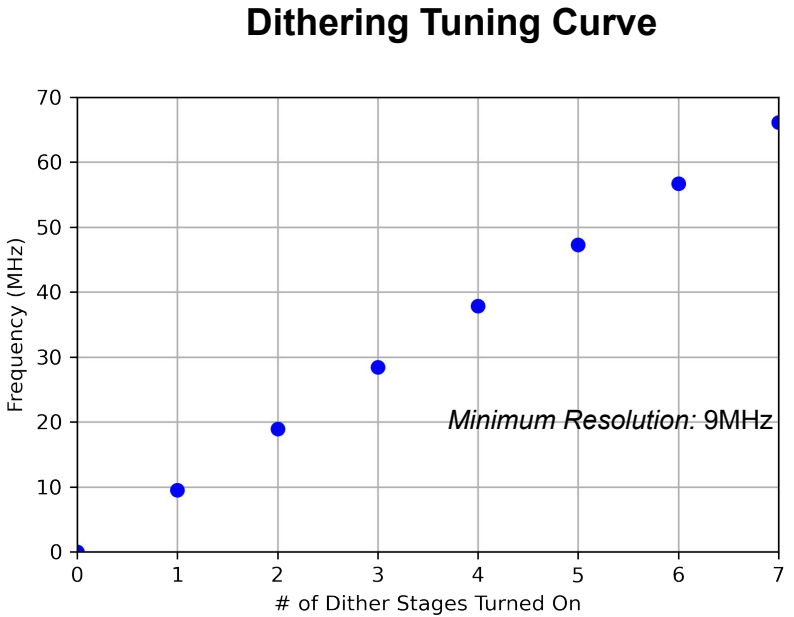
- Array of interconnected C2MOS ring oscillators
- Fixed capacitive load with variable drive strength
- 16X baseline is always on
- *Coarse control* through enabling rows
  - 255 rows, 8-bit control
  - Implemented using binary encoding for ease of simulation
  - In practice, thermometer encoding would be used
- *Fine control* through enabling individual dithering cells
  - 9.5MHz fine steps → ~9MHz output resolution
- Low power, lower frequency operation by simple scaling of supply voltage verified



DCO Measurements

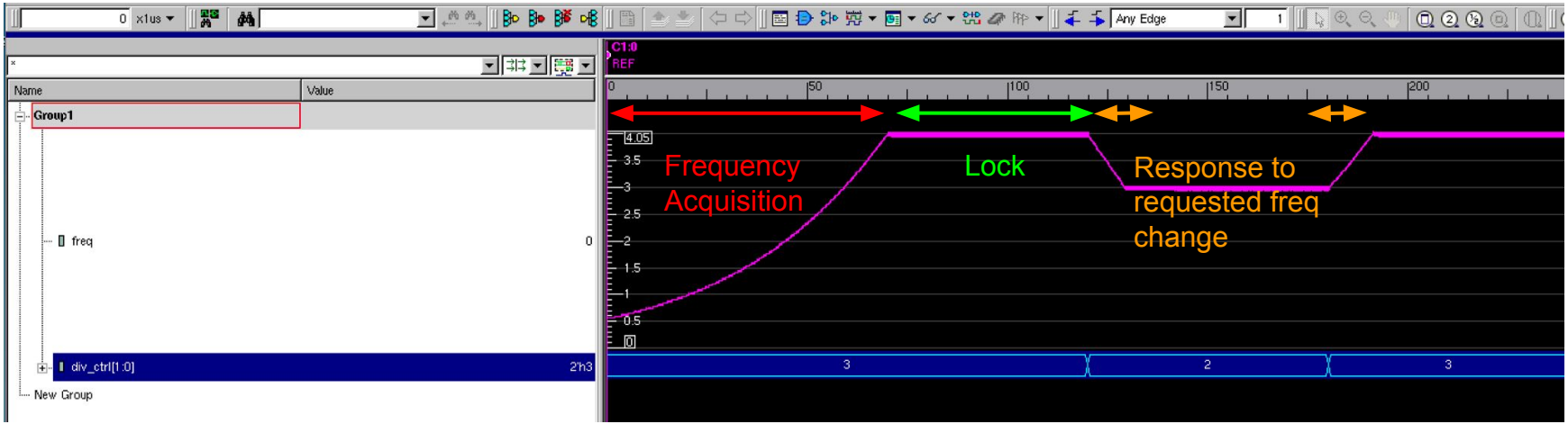
- Fine and coarse tuning shown to be highly linear





Dynamic PLL Operation

- Lock time from 4GHz → 3GHz: 9µs
- Pink curve represents output frequency

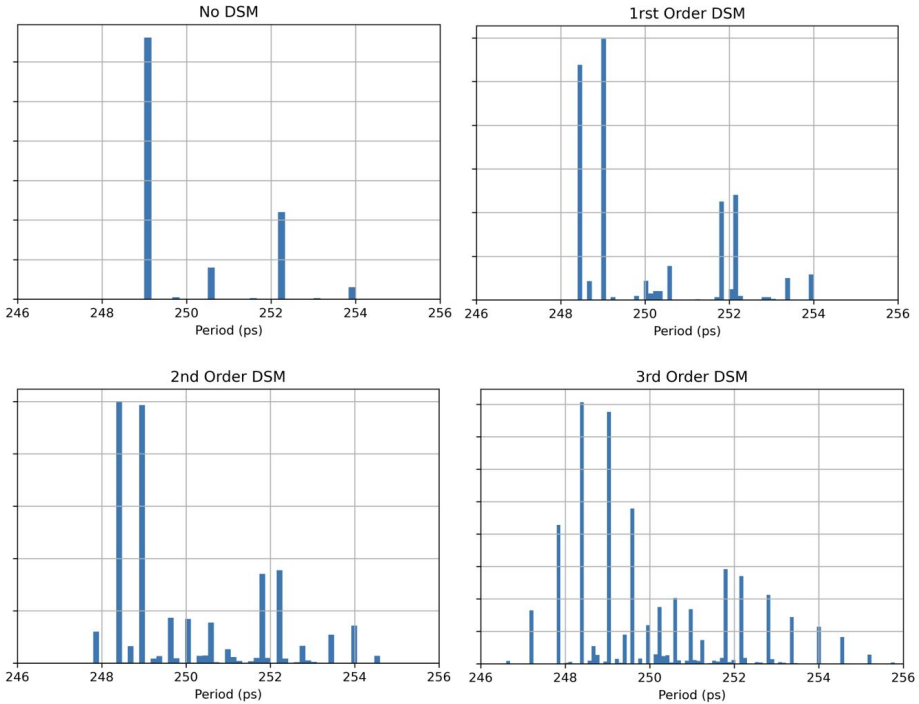


DSM Effect on Jitter and Resolution

- Higher order DSM → finer resolution, reduced spurs (spread spectrum)
- Also, increased jitter

DSM Order	Pk-to-Pk Jitter (ps)	RMS Jitter (ps)
0	5.00	1.54
1	5.60	1.70
2	6.80	1.76
3	9.20	1.87

Period Histograms for Different DSM Orders



Comparison with State of the Art

	Moore et al, 2018	Lin et al, 2015	Tierno et al, 2008	This work*
Process	14-nm	65-nm	0.18-μm	7-nm
Tuning Range (GHz)	1.0-5.5	0.5-8	0.25-1.367	0.5-7.239
RMS Period Jitter (ps)	1.29	0.7 @4GHz	8.884 @1.25GHz	1.76 @4GHz
PK-Pk Jitter (ps)	-	-	32.5 @1.25GHz	6.80 @4GHz
Locking Time (μs)	-	-	2.9	9
Power (mW)	9.7	15.6 @4GHz	35 @1.25GHz	2.3 @7.24GHz
Area (mm^2)	0.009	0.03	0.7735	0.0016

*Reported results are for the PLL architecture using the second-order DSM and nominal supply.

Next Steps

Improve Locking Time

- Dynamic Loop Bandwidth Adjustment
  - *Out of lock*: high bandwidth → fast loop response
  - *In lock*: low bandwidth → minimize steady state error
- Control word search algorithm

Full Compatibility with Digital Flow

- Integrate DCO into digital flow
- Investigate effects of P&R on performance
- Implement on-chip calibration scheme to compensate

Questions?

Acknowledgements and References

Big thanks to Wahid Rahman for sharing his C2MOS layout with us, helping us to understand dithering, and giving us simulation advice!

1. “File:Michelangelo's David - Floyd-Steinberg.png,” Wikimedia Commons, Sept. 2007. [Online]. Available: https://commons.wikimedia.org/wiki/File:Michelangelo%27s_David_-_Floyd-Steinberg.png
2. J. Lin and C. Yang, "A Fast-Locking All-Digital Phase-Locked Loop With Dynamic Loop Bandwidth Adjustment," *in IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 10, pp. 2411-2422, Oct. 2015.
3. J. A. Tierno, A. V. Rylyakov and D. J. Friedman, "A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 42-51, Jan. 2008.
4. D. M. Moore, T. Xanthopoulos, S. Meninger and D. D. Wentzloff, "A 0.009 mm2 Wide-Tuning Range Automatically Placed-and-Routed ADPLL in 14-nm FinFET CMOS," in *IEEE Solid-State Circuits Letters*, vol. 1, no. 3, pp. 74-77, Mar. 2018.