# EE 240B Final Project Report

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*Abstract*

In this report, I demonstrate the operation of a switched-capacitor ("SC") gain stage making use of an inverting switch architecture and two-stage operational transconductance amplifier ("OTA") that achieves the desired gain of 2 with 64.74 dB dynamic range, 0.1% dynamic settling error, and 0.1% static settling error.

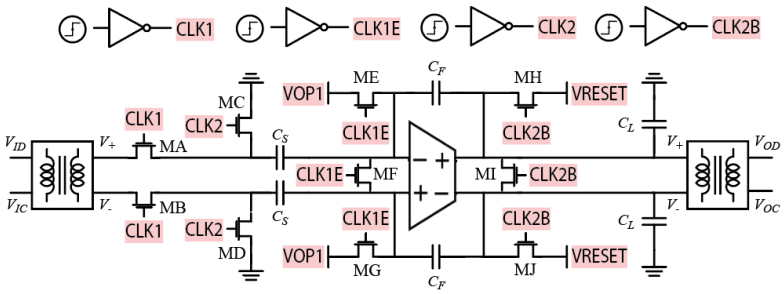



Figure 1: Selected SC topology, with buffered clock generation from ideal pulse voltage sources indicated at the top

*Design Procedure and Modeling*

To begin, I made the fairly straightforward decision to base the SC topology of my design on the single-ended inverting topology covered in class, primarily because its use of the technique of bottom-plate sampling allows for near complete nullification of potential charge injection and clock-feedthrough sampling error when used in a differential configuration. I also included the VOP1 and VRESET voltage sources to bias the OTA correctly for linear operation, as well as switches between the differential input and output lines for the CLK1E and CLK2B clocks to zero out differential charge while resetting these common-mode voltages.

Given that the desired closed-loop gain of the circuit is 2, and the analytic expression for this gain is $\frac{C_S}{C_F}$, this ratio is set at 2 from the offset. I selected $C_F$ to be 1 pF and $C_S$ to be 2 pF semi-arbitrarily, since I expected a feedback capacitance on the order of pF to cause negligible sampling noise (compared to that of the amplifier).

In feedback, the magnitude of the static settling error is approximately $\frac{1}{T_0}$, where $T_0$ is the DC loop gain. As a result, in order to achieve a static settling accuracy within the 0.25% requested by the project specification, the DC loop gain must be at least 400. The feedback factor, $\beta$, of this circuit is $\frac{C_F}{C_F+C_S+C_{in}}$, where $C_{in}$ is the parasitic capacitance of the OTA input devices. Since $C_F + C_S \gg C_{in}$, $\beta$ reduces to approximately $\frac{C_F}{C_F+C_S} = \frac{1}{3}$. As the DC loop gain is simply the product of the feedback factor and the DC gain of the OTA, this yields the concrete constraint that the OTA needs to achieve a DC gain greater than 1200 to meet the static settling error specification.

The dynamic settling error and sampling clock frequency specifications then determine the unity gain frequency of the OTA in feedback. Assuming a 50% duty cycle for the 150 MHz sampling clock, the time allocated for settling, $t_s$, is set at $\frac{1}{150\ MHz} * \frac{1}{2} = 3.33\ ns$. Now, accounting for the right half-plane zero present in the model for the evaluation phase (corresponding to CLK2) of this circuit, the settling time is also constrained by the following equation:

$$t_s = -\tau \ln\left(\epsilon_d\left(1 - \beta\left(\frac{C_f}{C_f + C_L}\right)\right)\right)$$

Assuming use of the minimum load capacitance of 200 fF, this yields the necessary time constant of the feedback, which in turn reveals the necessary unity gain frequency of the feedback loop.

$$\tau = -\frac{t_s}{\ln\left(\epsilon_d\left(1 - \beta\left(\frac{C_f}{C_f + C_L}\right)\right)\right)} = \frac{-3.33\ ns}{\ln\left((0.0025)\left(1 - \left(\frac{1}{3}\right)\left(\frac{1\ pF}{1\ pF + 200\ fF}\right)\right)\right)} = 0.528\ ns$$

$$f_u = \frac{1}{2\pi\tau} = 286\ MHz$$

This also sets a lower bound on the $G_m$ of the OTA, since $f_u$ is equivalent to the effective $G_m$ seen at the output divided by the effective capacitance seen at the output.

$$f_u = \frac{G_{m,eff}}{C_{Ltot}} = \frac{\beta G_m}{C_{Ltot}} \rightarrow G_m \geq \frac{f_u C_{Ltot}}{\beta} = \frac{f_u(C_L + (1-\beta)C_F)}{\beta} \approx 5\ mS$$

In order to meet these requirements, I chose to design a Miller-compensated, two-stage OTA. I selected the telescopic cascode topology for the first stage of my OTA and a simple common source configuration for the second stage. This second stage provided a decent transconductance boost, since the overall OTA $G_m$ became $g_{m2}A_{v1}$, where $g_{m2}$ is that of the second stage and $A_{v1}$ is the relatively high voltage gain of the telescopic first stage. Additionally, using this stage at the output ensured that there would be more output swing available than just about any single-stage solution, which was quite important for a good dynamic range.

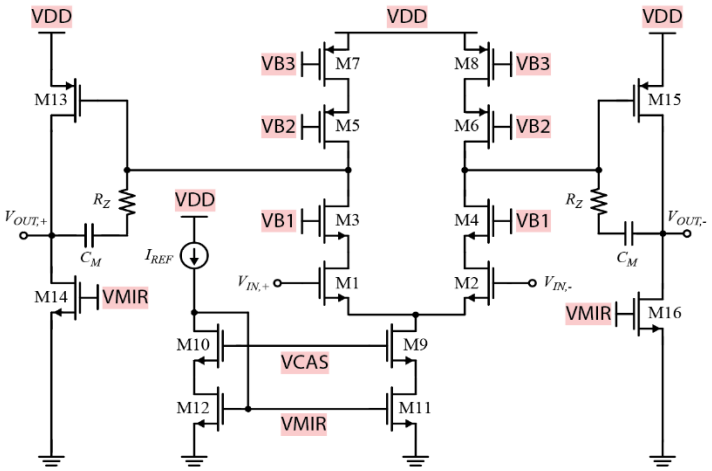



Figure 2: Schematic of OTA, numerical values for all components and biases and provided in Tables 2 and 3; note that VMIR is set by the wide-swing diode connection of M12, rather than by an external voltage.

*Noise Considerations*

Selecting this topology for the OTA had clear benefits from a dynamic range perspective, the most prominent of which is that the output swing and, accordingly, the maximum rms output signal, is high. However, introducing a Miller compensation capacitor $C_M$ completely altered the expression for the OTA's contribution to the total integrated output noise from that of a single-stage OTA, and placed this capacitance in the dominant position for determining the circuit's dynamic range overall.

$$v_{OT,G_m}^2 = \frac{kT}{\beta} * \frac{\gamma\alpha_1}{C_M}\left(1 + \beta\frac{\alpha_2 C_M}{\alpha_1 C_{Ltot}}\right)$$

Here, $k$ is the Boltzmann constant and $T$ is the temperature of the devices, taken in simulation to be 27° C, which is approximately 300 K. The value $\gamma$ is a process parameter that I verified empirically to be around 1 by running an AC sweep of the drain to source noise current of a typical device in the class's 65 nm process. As an additional consequence of this simulation, I verified that the flicker noise corner frequency of the devices I use in this project is around 17 MHz. This is not low enough to expect negligible total noise

contribution from this type of noise in simulation, but it is certainly low enough that mitigating this contribution is not a defining design consideration. The variables $\alpha_1$ and $\alpha_2$ are the noise factor coefficients for the first stage and the second stage, respectively. Referencing the device labeling in Figure 2, $\alpha_1 \approx 1 + V_1^*/V_7^*$, assuming that the cascode devices do not contribute significantly to the total noise, which is the case when the $f_T$ of the devices is more than 3 times larger than $f_u$. Without approximation, $\alpha_2 = 1 + V_{13}^*/V_{14}^*$.

Ignoring the effect of the resistances of the MOS switches (which I continued to do until simulation), the analytic expression for the total sampling noise of this topology was as follows.

$$v_{OT,samp}^2 = \frac{kT}{\beta} * \frac{1}{C_F}$$

This yielded the following expression for the total integrated voltage noise at the differential output of the circuit:

$$v_{OT}^2 = v_{OT,samp}^2 + v_{OT,G_m}^2 = \frac{kT}{\beta}\left(\frac{1}{C_F} + \frac{\gamma\alpha_1}{C_M} + \frac{\beta\gamma\alpha_2}{C_{Ltot}}\right)$$

For typical values of these parameters, it was clear that $C_M$ is the primary "controller" of noise in this circuit, with $C_{Ltot}$ making a smaller contribution due to the impact of $\beta$, and the contribution of $C_F$ small when chosen on the order of pF. It was therefore sufficient to keep $C_L$ at the minimum 200 fF, and thereby fix $C_{Ltot}$ at around 870 fF.

*Design Implementation*

To achieve the design illustrated in Figures 1 and 2, I first used Prof. Murmann's MATLAB script and simulation tables to plot $g_m r_o$ against $V^*$ for a number of channel lengths, as well as $f_T$ versus $V^*$ for these same channel lengths. Qualitatively, I determined that using a channel length of 110 nm for my OTA devices would give the best return in intrinsic gain while maintaining $f_T$ at around 30 GHz, which would prevent noise from cascode devices from affecting the amplifier's dynamic range. In the broader circuit, I assigned the switching devices the minimum channel length of 65 nm, since they do not provide gain.

Using the results of the $g_m r_o$ versus $V^*$ simulation described above, I selected a $V^*$ of 125 mV for the amplifying devices in the first stage of the OTA, and implemented this by using individualized testbenches to match $V^*$ to $V_{GS}$ for fixed $W$, $V_{DS}$, and $V_{BS}$ . The multiplier on $W$ was then scaled to achieve the desired drain current.

I began by arbitrarily setting the current in the first stage to be around 300 $\mu$A. However, I later scaled this to around 600 $\mu$A (by proportionally increasing the multipliers on the widths of the amplifier and tail current source devices) to ensure that slewing through the 550 fF compensation capacitor that I selected to control noise would not set the OTA slew rate. To implement this tail current, I made use of the wide-swing cascode current mirror topology, since it allowed decent current matching between the reference and tail currents and allowed me to achieve this without using overly large channel lengths. This made sizing the current source devices in the second stage much easier. I selected a $V^*$ of around 125 mV for these devices as well, although I set them to operate with $V_{DS}$ around 100 mV to lower their impact on the headroom of the first stage. Headroom did not end up as a constraining factor however, due to the gain of the second stage and corresponding small swing at the second stage input, so I could have allowed the tail devices more "room to breathe", so to speak.

To set the gate biases of the transconducting second stage devices (M13 and M15), I raised the voltage bias point of the output of the first stage until these devices achieved a reasonably low $V^*$ of 130 mV. Because the second stage current sources took on the $V^*$ of 125 mV from the current mirror, the transconducting

devices required a similar $V^*$ to minimize $\alpha_2$. I set the second stage current source transistors to sink slightly less than 750 $\mu$A to set a maximum slew rate of $\frac{I_{B2}}{C_M+C_{Ltot}} \approx 0.518\, V/ns$ .

Although $f_u$ under the Miller compensation scheme should have been approximately $\beta\frac{g_{m1}}{C_M} \approx 400\, MHz$, where $g_{m1}$ is that of the first stage (measured to be around 4 mS), the Miller right half-plane zero pushed it out in practice at the expense of the loop phase margin. I had initially added and tuned the zero-nulling resistor $R_Z$ to 900 Ω to achieve an $f_u$ of around 500 MHz and phase margin of 70° with $C_M$ set to 400 fF. However, I eventually realized that increasing $C_M$ to decrease total output noise, and thereby trading off on phase margin for $f_u$ , was definitely worthwhile, since even a feedback loop with a relatively low phase margin would settle relatively quickly with a small enough $\tau$. With $C_M$ set to 550 fF, the OTA achieved an $f_u$ of just under 1 GHz and phase margin of around 40°, allowing my design to easily meet the dynamic settling requirement.

*Performance Summary and Simulation Results*

After finalizing my design, I arrived at (or used simulation results to extract) the following values for the parameters relevant to the total output noise: $\gamma \approx 1, \beta \approx 0.33, \alpha_1 \approx 2, \alpha_2 \approx 2.04, C_M = 550\, fF, C_F = 1\, pF$, and $C_{Ltot} \approx 870\, fF$. I used these values to find the expected total output noise variance and dynamic range for a chosen output of 1 V (and differential input of 500 mV):

$$v_{OT}^2 = \frac{kT}{\beta}\left(\frac{1}{C_F}+\frac{\gamma\alpha_1}{C_M}+\frac{\beta\gamma\alpha_2}{C_{Ltot}}\right) \approx 6.79 * 10^{-8}\, V^2 \rightarrow N_{OT,rms} \approx 260.62\, \mu V$$

$$DR = 10\log_{10}(v_O^2/v_{OT}^2) = 10\log_{10}(1\, V^2/(6.79 * 10^{-8}\, V^2)) = 71.68\, dB$$

After running a periodic steady-state and periodic noise simulation with maximum AC frequency and maximum sideband settings at values with convergent total noise results and relatively small input of 50 mV, the total rms integrated output noise came out to 579.18 $\mu$V. This is quite a bit higher than the expected value, but it's possible that flicker noise and noise from the cascode devices factored in more significantly than I predicted. In any case, the resultant dynamic range is 64.74 dB, which still meets the design specification.

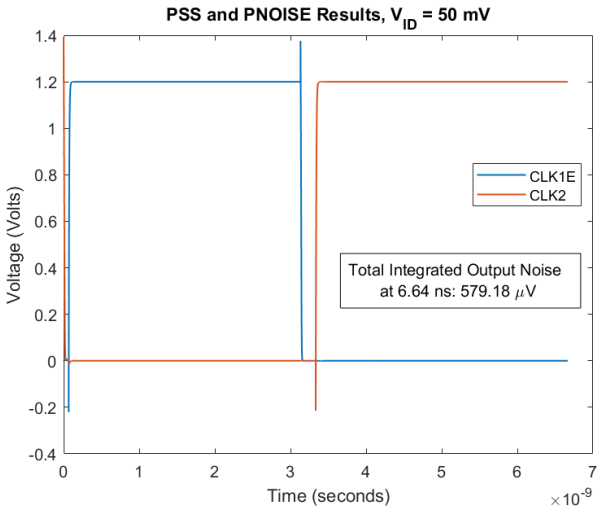
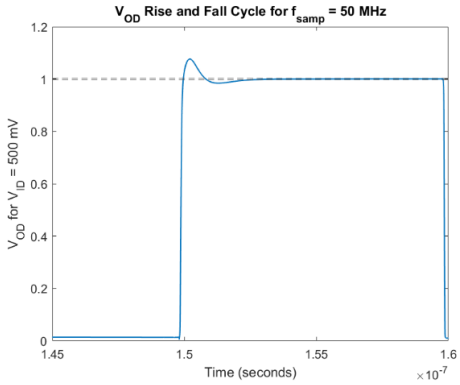


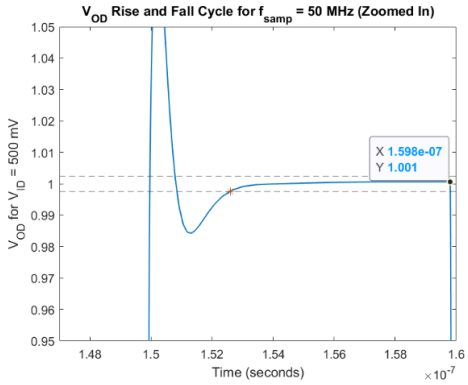

Figure 7: Periodic steady-state (PSS) and periodic noise (PNOISE) simulation results, with rms total integrated output noise near the end of the evaluation phase

To verify static settling accuracy, I set the sampling frequency of the system to 50 MHz to give the output a relatively long time to settle to a final value. As can be seen in Figures 3 and 4, the approximate final settling point for an input of 500 mV is 1.001 V. The static settling error is therefore $\frac{1.001-1}{1} = 0.1\%$. This is quite a bit higher than the expected value of about $\frac{1}{7800} = .013\,\%$, but it's likely that a gradually changing output common-mode voltage introduced additional error to this measurement. I elaborate on this in the final section.

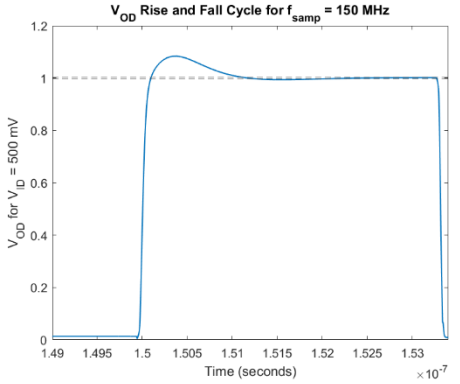
I then increased the sampling frequency back to 150 MHz in order to verify sufficient dynamic settling within the allotted time. Here, the output settled to 1.002 V for a 500 mV input, meaning that the dynamic

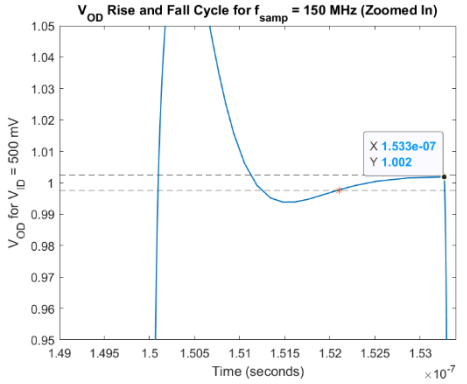
settling error is $\frac{1.002-1.001}{1.001} = 0.1\,\%$. The changing output common-mode issue seemed to affect this measurement as well, which can be seen in the slightly different settling curve.




Figures 3 and 4: Measurement of static settling error using a sampling frequency of 50 MHz; convergence of output error within 0.25% is shown at the red asterisk




Figures 5 and 6: Measurement of dynamic settling error using the original sampling frequency of 150 MHz; convergence of output error within 0.25% is shown at the red asterisk

I measured the static power dissipated by the OTA by running a DC operating point simulation. With a reference current of 150 $\mu$A, the exact first stage tail current is 590.7 $\mu$A and the two second stage currents are each 735.7 $\mu$A. The static power dissipation is therefore $(1.2\,V) * (150\,\mu\text{A} + 590.7\,\mu\text{A} + 2 * 735.7\,\mu\text{A}) = 2.65\,mW$. Finally, I measured the dynamic power dissipation of the clock buffers as $P_{dyn} = V_{DD}I_{avg} = (1.2\,V) * (0.3117\,A) = 374\,mW$. This is quite high, which means that my design of the inverters and switches, which was done as a last step, likely needed to be much better thought-out.

Table 1: Performance Summary

| ***Design Parameter*** | **Specification** | **Actual** |
|---|---|---|
| *Closed-Loop Amplifier Gain* | 2 | 2 |
| *Output Dynamic Range* | 60 dB | 64.74 dB |
| *Static Settling Error* | <0.25% | 0.1% |
| *Dynamic Settling Error* | <0.25% | 0.1% |
| *Sampling Clock Frequency* | 150 MHz | 150 MHz |
| *OTA Static Power Dissipation* | Minimum | 2.65 mW |
| *Buffer Dynamic Power Dissipation* | Minimum | 374 mW |

*Component and Biasing Summary*

Tables 2 and 3: Component and Biasing Summary

| ***Transistor(s)*** | **L** | **W** | **Multiplier** |
|---|---|---|---|
| MA, MB, MC, MD, ME, MG | 65 nm | 1 $\mu$m | 40 |
| MH, MI, MJ | 65 nm | 1 $\mu$m | 250 |
| MF | 65 nm | 1 $\mu$m | 20 |
| INVERTER NMOS | 65 nm | 1 $\mu$m | 10 |
| INVERTER PMOS | 65 nm | 1 $\mu$m | 27 |
| M1, M2, M3, M4 | 110 nm | 1 $\mu$m | 20 |
| M5, M6, M7, M8 | 110 nm | 1 $\mu$m | 110 |
| M13, M15 | 110 nm | 1 $\mu$m | 460 |
| M14, M16 | 110 nm | 1 $\mu$m | 170 |
| M9, M11 | 110 nm | 1 $\mu$m | 170 |
| M10, M12 | 110 nm | 1 $\mu$m | 43 |

| ***Component / Bias*** | **Value** |
|---|---|
| $C_M$ | 550 fF |
| $R_Z$ | 900 Ω |
| $C_S$ | 2 pF |
| $C_F$ | 1 pF |
| $C_L$ | 200 fF |
| $I_{REF}$ | 150 $\mu$A |
| *VIC* | 0 V |
| *VDD* | 1.2 V |
| *VB1* | 821 mV |
| *VB2* | 645.9 mV |
| *VB3* | 790.5 mV |
| *VCAS* | 475.1 mV |
| *VOP1* | 675 mV |
| *VRESET* | 300 mV |

*Design Critique*

Throughout my design process I attempted to calculate all values methodologically, in the style presented in lecture. However, I faced many difficulties in translating Prof. Boser's design approach to this project. A few examples of this include erroneously using the noise equations for an uncompensated, single-stage OTA and using a sinusoidal model for the output signal variance. I was lucky that the latter error (multiplying the true output signal variance by 1/8) compensated in part for the former error, which represented a gross mischaracterization and underestimation of the total output noise.

In addition, I faced a lot of "real world" issues in getting my design to work in simulation. If I was completing this design in a professional context, I would have dedicated a lot more time to correctly sizing the clock buffers and switches to avoid the incredibly large dynamic power penalty that my current implementation incurs. Beyond this, I would have also investigated the steadily changing output common mode issue that affected my settling error measurements. During transient simulation, one or the other of the OTA outputs would shift toward VDD or ground across clock cycles. It was difficult to diagnose the cause of this in the time allotted for this design – I verified that my OTA's CMRR was around 228 dB, which should have helped mitigate an issue like this. Given more time, I hopefully would have been able to fix this.